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ON-CHIP INDUCTANCE IN HIGH SPEED INTEGRATED CIRCUITS

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Resumo de On-Chip Inductance in High Speed Integrated Circuits

The appropriate interconnect model has changed several times over the past two decades due to the application of aggressive technology scaling. New, more accurate interconnect models are required to manage the changing physical characteristics of integrated circuits.

Currently, RC models are used to analyze high resistance nets while capacitive models are used for less resistive interconnect. However, on-chip inductance is becoming more important with integrated circuits operating at higher frequencies, since the inductive impedance is proportional to the frequency.

The operating frequencies of integrated circuits have increased dramatically over the past decade and are expected to maintain the same rate of increase over the next decade, approaching 10 GHz by the year 2012.

Also, wide wires are frequently encountered in important global nets, such as clock distribution networks and in upper metal layers, and performance requirements are pushing the introduction of new materials for low resistance interconnect, such as copper interconnect already used in many commercial CMOS technologies.

On-Chip Inductance in High Speed Integrated Circuits deals with the design and analysis of integrated circuits with a specific focus on on-chip inductance effects. It has been described throughout this book that inductance can have a tangible effect on current high speed integrated circuits.

For example, neglecting inductance and using an RC interconnect model in a production 0.25 mum CMOS technology can cause large errors (over 35%) in estimates of the propagation delay of on-chip interconnect.

It has also been shown that including inductance in the repeater insertion

design process as compared to using an RC model improves the overall repeater solution in terms of area, power, and delay with average savings of 40.8%, 15.6%, and 6.7%, respectively.

On-Chip Inductance in High Speed Integrated Circuits is full of design and analysis techniques for RLC interconnect. These techniques are compared to techniques traditionally used for RC interconnect design to emphasize the effect of inductance.

On-Chip Inductance in High Speed Integrated Circuits will be of interest to researchers in the area of high frequency interconnect, noise, and high performance integrated circuit design.